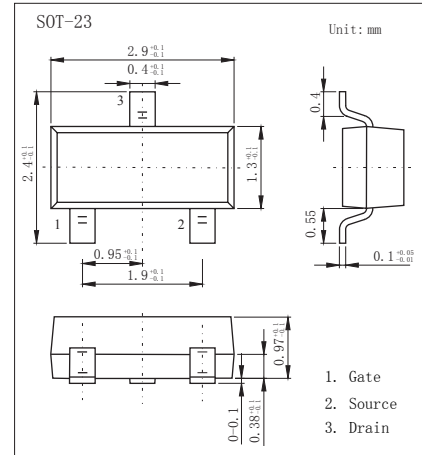
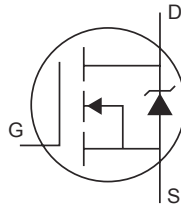


N-Channel MOSFET

IRLML2402

■ Features

- $V_{DS} (V) = 20V$
- $I_D = 1.2 A (V_{GS} = 4.5V)$
- $R_{DS(ON)} < 250m\Omega (V_{GS} = 4.5V)$
- $R_{DS(ON)} < 350m\Omega (V_{GS} = 2.7V)$


■ Absolute Maximum Ratings $T_a = 25^\circ C$

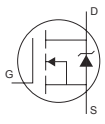
| Parameter | Symbol | Rating | Unit | |
|---|------------|------------------|----------------|---|
| Drain-Source Voltage | V_{DS} | 20 | V | |
| Gate-Source Voltage | V_{GS} | ± 12 | | |
| Continuous Drain Current | I_D | $T_A=25^\circ C$ | 1.2 | A |
| | | $T_A=70^\circ C$ | 0.95 | |
| Pulsed Drain Current | I_{DM} | 7.4 | | |
| Power Dissipation | P_D | 540 | mW | |
| Linear Derating Factor | | 4.3 | mW/ $^\circ C$ | |
| Peak Diode Recovery dv/dt (Note.1) | dv/dt | 5 | V/ns | |
| Thermal Resistance Junction- to-Ambient | R_{thJA} | 230 | $^\circ C/W$ | |
| Junction Temperature | T_J | 150 | $^\circ C$ | |
| Storage Temperature Range | T_{stg} | -55 to 150 | | |

Note.1: $I_{SD} \leq 0.93A$, $di/dt \leq 90A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ C$

N-Channel MOSFET

IRLML24 02

■ Electrical Characteristics Ta = 25°C

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---------------------------------------|---------------------|--|-----|------|------|------|
| Drain-Source Breakdown Voltage | V _{DSS} | I _D =250 μA, V _{GS} =0V | 20 | | | V |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{DS} =16V, V _{GS} =0V | | | 1 | μA |
| | | V _{DS} =16V, V _{GS} =0V, T _J =125°C | | | 25 | |
| Gate-Body Leakage Current | I _{GSS} | V _{DS} =0V, V _{GS} =±12V | | | ±100 | nA |
| Gate Threshold Voltage | V _{GS(th)} | V _{DS} =V _{GS} , I _D =250 μA | 0.7 | | 1.5 | V |
| Static Drain-Source On-Resistance | R _{DS(on)} | V _{GS} =4.5V, I _D =0.93A (Note.1) | | | 250 | mΩ |
| | | V _{GS} =2.7V, I _D =0.47A (Note.1) | | | 350 | |
| Forward Transconductance | g _{FS} | V _{DS} =10V, I _D =0.47A | 1.3 | | | S |
| Input Capacitance | C _{iss} | V _{GS} =0V, V _{DS} =15V, f=1MHz | | 110 | | pF |
| Output Capacitance | C _{oss} | | | 51 | | |
| Reverse Transfer Capacitance | C _{rss} | | | 25 | | |
| Total Gate Charge | Q _g | V _{GS} =16V, V _{DS} =4.5V, I _D =0.93A (Note.1) | | 2.6 | 3.9 | nC |
| Gate Source Charge | Q _{gs} | | | 0.41 | 0.62 | |
| Gate Drain Charge | Q _{gd} | | | 1.1 | 1.7 | |
| Turn-On DelayTime | t _{d(on)} | V _{DS} =10V, I _D =0.93A, R _D =11Ω, R _G =6.2Ω (Note.1) | | 2.5 | | ns |
| Turn-On Rise Time | t _r | | | 9.5 | | |
| Turn-Off DelayTime | t _{d(off)} | | | 9.7 | | |
| Turn-Off Fall Time | t _f | | | 4.8 | | |
| Body Diode Reverse Recovery Time | t _{rr} | I _F = 0.93A, dI/dt= 100A/μs, T _J = 25°C (Note.1) | | 25 | 38 | nC |
| Body Diode Reverse Recovery Charge | Q _{rr} | | | 16 | 24 | |
| Maximum Body-Diode Continuous Current | I _S | MOSFET symbol showing the integral reverse p-n junction diode.  | | | 0.54 | A |
| Pulse Source Current (Body Diode) | I _{SM} | | | | 7.4 | |
| Diode Forward Voltage | V _{SD} | I _S =0.93A, V _{GS} =0V, T _J = 25°C (Note.1) | | | 1.2 | V |

Note.1: Pulse width ≤ 300μs; duty cycle ≤ 2%.

■ Marking

| | |
|---------|------|
| Marking | 1A** |
|---------|------|

N-Channel MOSFET
IRLML2402

■ Typical Characteristics

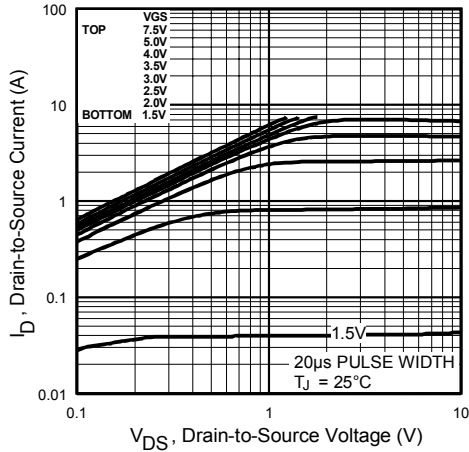


Fig 1. Typical Output Characteristics

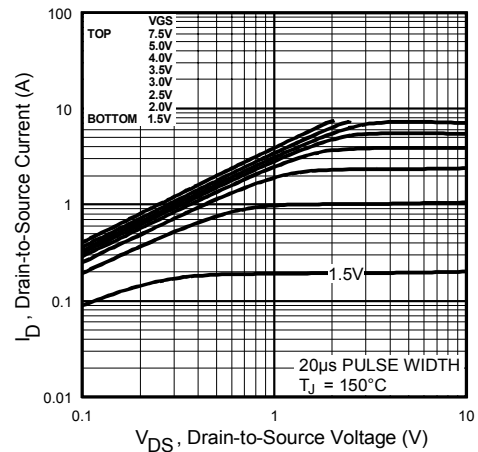


Fig 2. Typical Output Characteristics

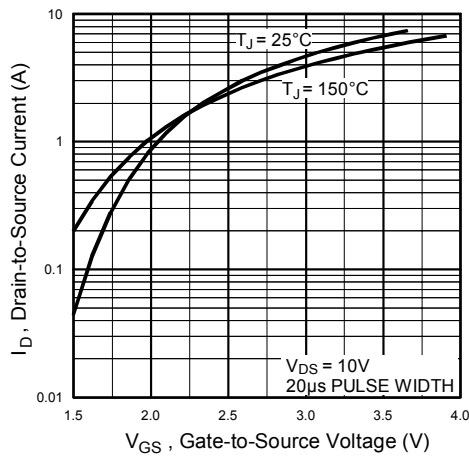


Fig 3. Typical Transfer Characteristics

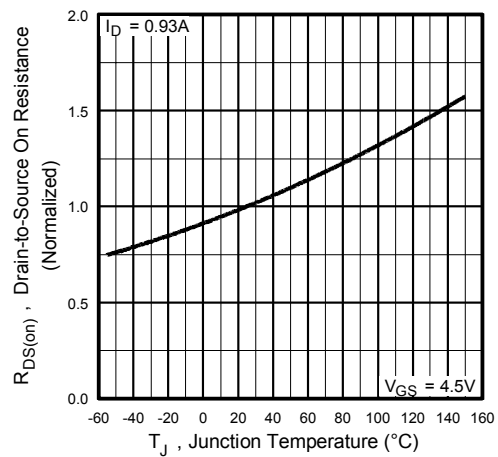


Fig 4. Normalized On-Resistance Vs. Temperature

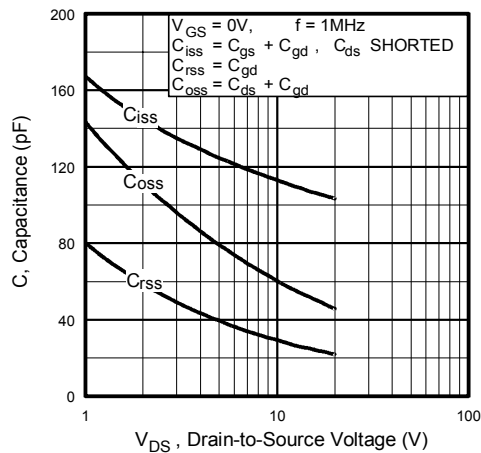


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

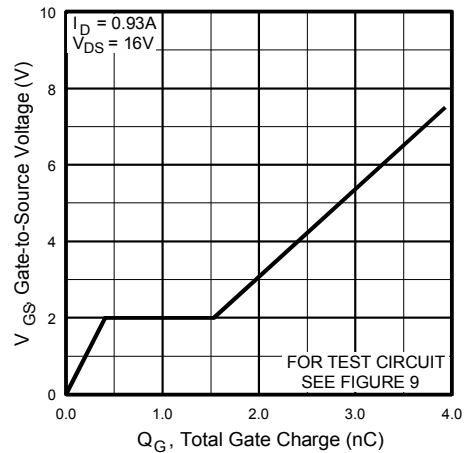


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

N-Channel MOSFET
IRLML2402

■ Typical Characteristics

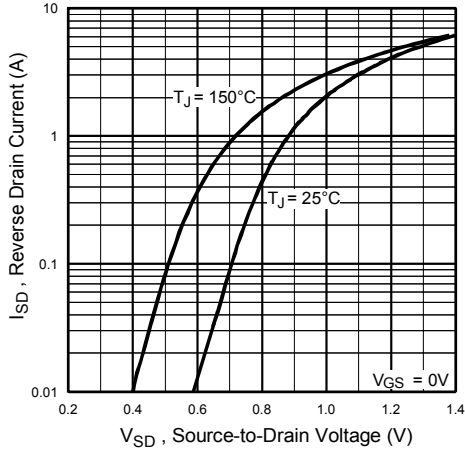


Fig 7. Typical Source-Drain Diode Forward Voltage

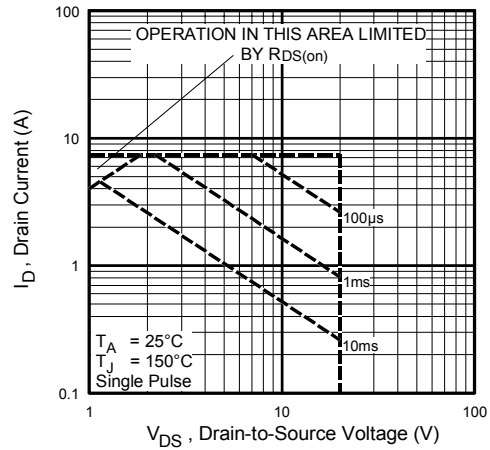


Fig 8. Maximum Safe Operating Area

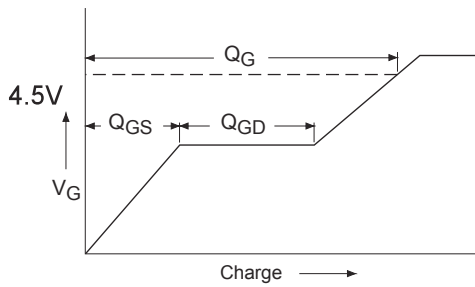


Fig 9a. Basic Gate Charge Waveform

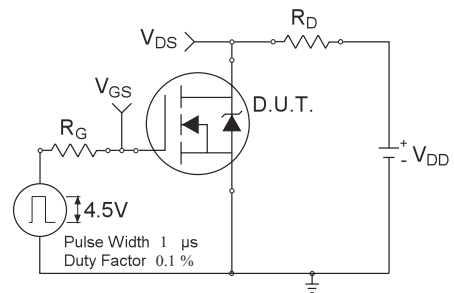


Fig 10a. Switching Time Test Circuit

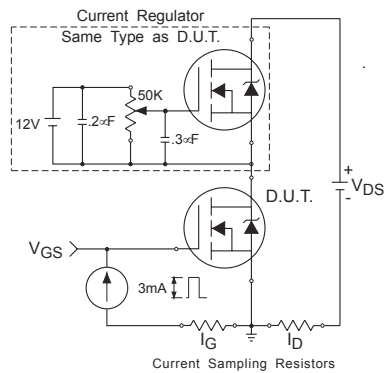


Fig 9b. Gate Charge Test Circuit

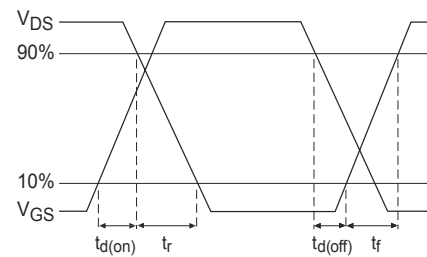


Fig 10b. Switching Time Waveforms

N-Channel MOSFET IRLML2402

Typical Characteristics

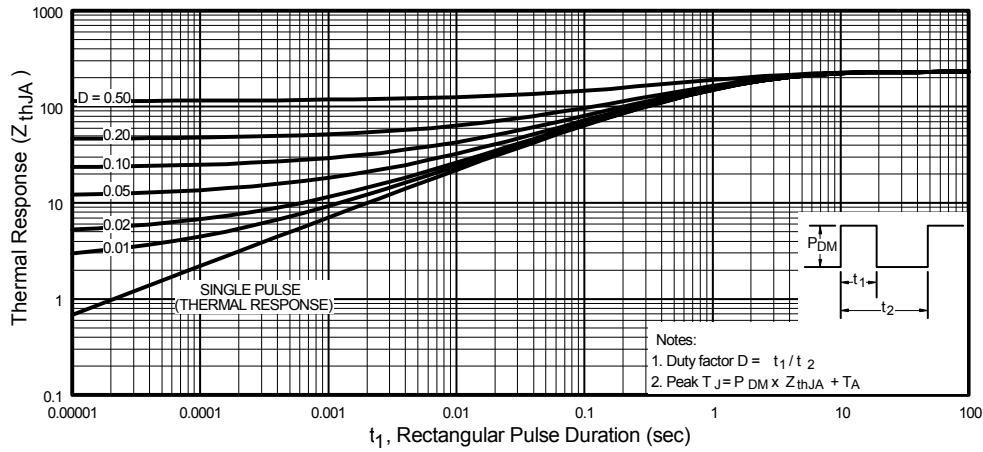
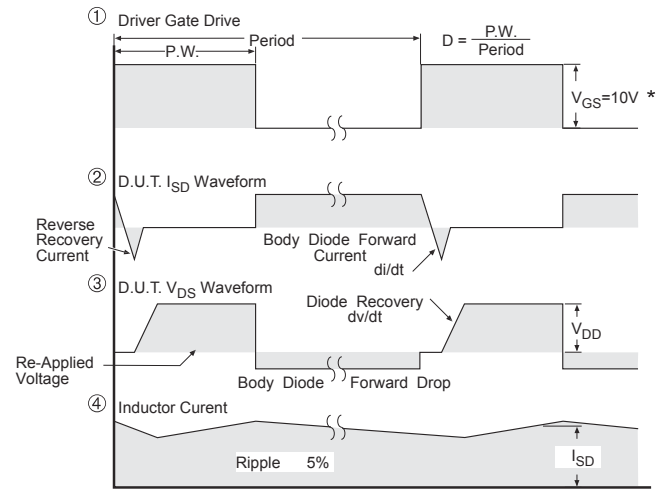
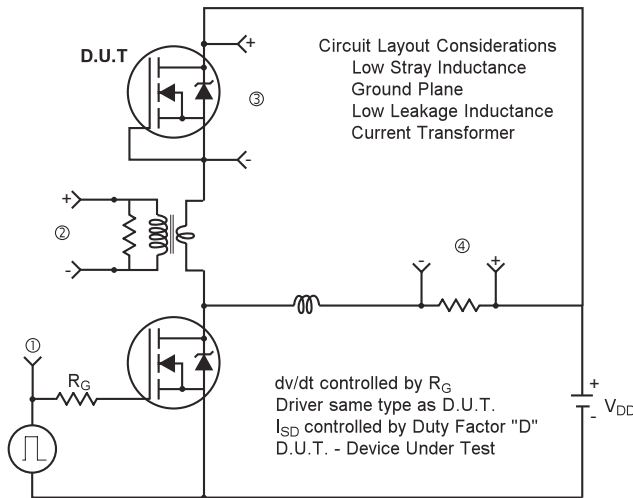


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

Fig 12. For N-Channel HEXFETS